REMARKS

This is in response to the Office Action mailed on November 17, 2004, and the references cited therewith. Claims 1, 9, 11-12, 14, 20 are amended, no claims are canceled or added; as a result, claims 1-23 are now pending in this application. Reconsideration of the application is respectfully requested.

§103 Rejection of the Claims

Claims 1-11 and 20-23 were rejected under 35 USC § 103(a) as being unpatentable over Rhee et al. (U.S. Patent No. 6,147,561) in view of Suzuki et al. (U.S. Patent No. 5,258,626).

Claims 14-19 were rejected under 35 USC § 103(a) as being unpatentable over Rhee et al. (U.S. Patent No. 6,147,561) and Suzuki et al. (U.S. Patent No. 5,258,626) as applied to claims 1-10 and 20-22 above, and further in view of Carr (U.S. Patent No. 6,377,315).

Applicant's claims 1 - 11 are directed to a low phase-noise oscillator that generates a reference frequency as its output. The reference frequency is not phase locked and may be changed based on the amount of phase shift applied by the phase shifter. Rhee, on the other hand, discloses a phase-locked-loop (PLL) that uses a reference frequency as its input (see FIG. 2 of Rhee, reference designation #10) to provide a phase-locked frequency output. Applicant's generated reference frequency output may be used, for example, as Rhee's reference frequency input. The operation and configuration of Applicant's claimed low phase-noise oscillator is very different than Rhee's PLL. For example:

1) Rhee's phase detector #14 compares time-delayed/phase shifted signals generated from an input reference frequency #10 with time-delayed/phase shifted signals generated from an output frequency #204. In other words, Rhee uses two different frequency sources as input to the phase detector. Applicant's phase detector, as recited in claim 1, compares a time-delayed reference with a phase-shifted reference from the same source (i.e., the frequency generator).

2) Rhee's phase shifters provide ninety-degree phase shifts (see FIG. 2 of Rhee, elements 200 and column 5, lines 22 – 31). Applicant's phase-shifted reference signal is not shifted by a predetermined amount, but the amount of phase-shift may be selected to set the output frequency. As recited in claim 1, during operation, the control signal causes the frequency generator to change its oscillation frequency to drive the phase difference between the low

phase-noise time-delayed reference signal and the phase-shifted reference signal to substantially ninety degrees. Therefore, the amount of phase shift of Applicant's phase shifted reference signal is determined by the frequency (which can change) and the amount of delay introduced by the delay element. This phase shift does not require any specific value.

3) Applicant's claim 1, as amended, also recites a variable phase shifter, and Applicant's claim 11, as amended, recites a signal splitter. These elements and their operation are not taught, suggested or motivated by Rhee. The variable phase shifter phase shifts the reference signal to generate the phase-shifted reference signal, and the signal splitter splits the reference signal from the frequency generator and provides the reference signal to both the phase shifter and delay element. In reference to Applicant's claim 1, one of the "split" reference signals is operated on by the high-temperature superconductor delay element before being is operated on by the variable phase shifter before being applied to the phase detector. As recited in claim 10, the phase shift provided by the variable phase shifter is selected to set the oscillation frequency. Rhee does not show a variable phase shifter nor does Rhee show a signal splitter that splits the same reference signal for applying to a phase detector. Rhee's phase detector #14 receives signals from different sources. Furthermore, Rhee's phase shifters #200 and #202 (see Rhee FIG. 2 and FIG. 10) provide only a fixed 90 degree phase shift.

Applicants further submit that Rhee's teachings, either separately or in combination with the other cited references, cannot result in a low noise frequency source, and furthermore that Rhee ***teaches away*** from low noise frequency generation. As discussed in more detail below, it will become apparent that Rhee's teachings actually increase the noise within the loop bandwidth, rather than reducing or canceling it.

In view of the above, Applicants submit that claims 1 – 11 are not taught, suggested or motivated by Rhee and are allowable over the cited references. Furthermore, Applicants submit that combining Rhee with either Suzuki and/or Carr does not result in Applicants' claimed invention.

Suzuki discloses a superconductive delay line. Applicants respectfully disagree with the Examiner's assertion that Suzuki's delay line is random. Suzuki's FIG. 5 clearly shows the delay line as a spiral. This pattern is a specific structure that will result in increased cross-coupling between the elements that increases noise. This structure may be unsuitable suitable for some

embodiments of Applicant's invention because of the induced noise. Applicants' delay element, as recited in claims 4, 13 and 17 is stated to be a random, meaning it has no specific pattern. A randomly arranged delay line will reduce the noise caused by cross coupling. Other delays lines, such as meandering delay lines may also provide low noise, and Applicants claims 1 – 3, 5 – 12, 14 – 16 and 20 – 23 are believed to cover delay lines of both random and non-random arrangements.

Applicant's claims 14 and 20, as amended, have similar recitations to amended claim 1 and are also believed to be allowable over the cited references based on the remarks above. Dependent claims 15 – 19 are also believed to be allowable at least because of their dependency on claim 14, and dependent claims 21 - 23 are also believed to be allowable at least because of their dependency on claim 20.

Discussion on Rhee's Increased Noise

Applicants submit that Rhee PLL ***teaches away*** from Applicants' low-noise frequency generation. Rhee discloses a general phase locked loop that uses a method to generate a higher gain digital phase detector. The output (Fout) is related to the to the reference frequency (Fref) by the equation: Fout=M*Fref/R. Consequently, the output is an integer multiple of the divided reference. The major difference between Rhee's design and a more conventional PLL design is the inclusion of three 90 degree phase shifts of the reference and divided down feedback signals (See Rhee FIG. 2). The net effect in Rhee is to generate a phase detector with a gain four times greater than is normally accomplished (with the added benefit that the reference sidebands are at four times the reference frequency). Other than this, classical phase locked loop analysis applies. Given this, the noise from the reference source is gained up (i.e., increased) to the output by the following equation: Nout=Nref+20*log(M/R) (the digital noise is gained by 20*log(M)). As can be seen, the noise of the reference signal is gained up by 20*log(M/R). As an example, assuming a reference noise at 5 KHz off of the carrier of -110 dBc/Hz, a reference divider of 10, and a feedback divider of 1000, the noise at the output of the loop would be –70 dBc/Hz at 5 KHz off the carrier (assuming that this is inside the loop bandwidth). Additionally, the digital noise would be gained up by 60 dB. If the reference were a 10 MHz crystal which was then multiplied to 1GHz in a PLL and then multiplied to 10 GHz through a step recovery diode multiplier, the noise

at 5 KHz offset would be –50 dBc/Hz (the noise is raised another 20 dB due to a factor of 10 multiplication). This does not even include the noise from the digital noise sources such as the reference and feedback dividers and phase detector. Thus, Rhee's teachings are adverse to the generation of a low noise frequency source.

Applicants' claims 1 - 11, on the other hand, may be viewed a discriminator with an automatic-frequency control (AFC) loop that may reduce the open loop, close-in noise of a frequency generator (e.g., a VCO, a DRO, a SAW, a Crystal, a L-C VCO, etc.). Unlike Rhee, the reference and feedback frequency in Applicants' claims are from the same source and the frequency generator may appear as an open loop component that will not necessary be frequency stable because there is no stable reference for it to be locked to.

Unlike Rhee, Applicants' delay element is used to decorrelate the frequency generator. The delay element delays a portion of the frequency generator so that by the time the signal reaches the phase detector (typically a mixer and not a digital device as in Rhee); the two signals are no longer correlated above some frequency. When this happens, the error signal (recited as the control signal) may degenerate a portion of the frequency generator's phase noise spectrum. The variable phase shifter is a tunable element that may be used to tune the degenerated frequency generator once the discriminator loop is closed. The specific phase shift value of the variable phase shifter is of no consequence as long as it has enough range to cover the range of interest. In some embodiments, recited in claim 9, for example, a SAW is used as the frequency generator because of its nose floor may be <-175 dBc/Hz at offsets greater than 50 KHz and the fact that the close-in noise is good (typically a good one is –145 dBc/Hz at 5 KHz offset). As can be seen, the SAW is already cleaner if multiplied to 10 GHz (-125 dBc/Hz) than using a standard PLL. However, in some applications (e.g., some receivers), a cleaner close-in source may be needed. Even though the above numbers are for a state of the art SAW VCO, Applicants' claimed invention may provide yet a further reduction in noise. In accordance with the teachings of Applicants' claim 1, the amount that the noise can be cleaned up may be a function of (1) delay line loss (signal to thermal noise ratio) (2) residual phase noise of the device (can become a limitation) (3) delay length (limits how close to the carrier can be degenerated). Given a delay of 5 to 10 uS, the open loop SAW may be cleaned up by approximately 20 to 25 dB from 1 KHz to 10 KHz. If 5 KHz is used as above, an open loop SAW VCO phase noise of –165 dBc/Hz may

result. When translated to 10 GHz, a noise of –145 dBc/Hz may result. This low-noise frequency generator, which may use a SAW VCO, a discriminator (i.e., splitter, delay element, tunable phase shifter, phase detector), and LPF is now a lower noise VCO with its output at the original SAW output and a new tune port at the tunable phase shifter input. This low-noise frequency generator may now be locked in a very narrow bandwidth loop (<100 Hz) to the same 10 MHz crystal as used in the Rhee example above. The loop alone with additional passive filtering may reject the noises by 5 KHz so that the SAW output will retain its spectral purity at 5 KHz. What has been accomplished is to generate a stable high frequency source that has high stability and lower close in (5 KHz in this case) phase noise than could be achieved by using an ordinary Phase Locked Loop or through physical multiplying. This is because, in a normal PLL, the close in noise of the base crystal will always be present and there is no way to filter it out. Fr example, the PLL increases the noise inside the loop bandwidth by 20*log(feedback division ratio), a physical multiplier increases the noise the same).

Allowable Subject Matter

Claims 12 and 13 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 12 has been amended to include the limitations of base claim 1 and intervening claims 9 through 11 and is therefore believed to be in condition for allowance. Claim 13 is believed to be allowable at least because of its dependency on claim 12.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney Gregory J. Gorrie (Reg. No. 36,530) at (480) 659-3314 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 50-0888.

Respectfully submitted,

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Date 2-2-05

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